REMARKS

Claims 1-8 and 26-37 will be pending upon entry of the present amendment. Claims 1, 3, 4, and 5 are amended and claims 26-37 are newly submitted with the present amendment.

In response to the Restriction Requirement issued by the Examiner on February 28, 2003, the applicant elected Species I, with traversal. In the Office Action of April 17, 2003, the Examiner acknowledges the applicant's election of species I. However, the Examiner has failed to reconsider the Restriction Requirement, as required in 37 C.F.R. § 1.143, and in Section 821.01 of the M.P.E.P., which reads "If, upon reconsideration, the Examiner is still of the opinion that restriction is proper, it should be repeated and made final in the next Office Action. In doing so, the Examiner should reply to the reasons or arguments advanced by applicants in their traverse."

Applicant respectfully requests that the Examiner reconsider the Restriction Requirement and, should the requirement be made final, provide a response to the applicant's arguments, which may be found in the Response to the Restriction Requirement filed on March 28, 2003.

The Examiner has objected to "the entire structure" as recited in claims 1, 3, 4, and 5. Accordingly, these claims have been amended to resolve this informality. A minor typographical error has also been corrected in claim 1. The amendment is not made to overcome any art, nor is the scope of the claims changed.

The Examiner has rejected claims 1-8 under 35 U.S.C. § 103(a) as being unpatentable over Background of Invention (BOI) in view of Ikemasu (5,693,970).

In rejecting claim 1, the Examiner has cited the art disclosed in the Background of the Invention as teaching the elements of the preamble of the claim, while acknowledging that the BOI fails to teach any of the limitations recited in the body of claim 1. The Examiner relies on Ikemasu for a teaching of all of the limitations of the body of the claim. However, Ikemasu fails to teach the limitations of claim 1 in several respects. The Examiner cites Ikemasu's SiO_2 film layers 16 and 17, and Si_3N_4 film layer 18 as being analogous to the first, second, and third insulating layers of claim 1, respectively. However, claim 1 recites depositing a second

insulating layer, selectively etchable with respect to the first insulating layer. Ikemasu's SiO_2 film layer 17, cited by the Examiner as corresponding to the second insulating layer, is not selectively etchable with respect to the SiO_2 film layer 16, which the Examiner has cited as corresponding to the first insulating layer of claim 1.

Furthermore, claim 1 recites etching the second insulating layer to only maintain it above the insulated conductive lines, at least above an active region of the substrate. Ikemasu provides no teaching to etch the SiO_2 film layer 17, while maintaining it above an insulated conductive line. While the Background teaches the formation of conductive lines, there is no teaching in the Background to deposit insulating layers, selectively etchable with respect to a layer beneath, nor is there any motivation in the Background of the Invention to combine the teachings of Ikemasu therewith to arrive at such a method, since the only suggestion of a benefit to such an arrangement is found in the applicant's own disclosure.

Additionally, the benefit disclosed by the applicant for using layers of selective etchability comes from etching the first and third layers using a chemistry to which the second layer is resistant. This provides a means for protecting the underlying wordlines from a short circuit in case of a misalignment of the opening formed (Figure 3C and page 8, lines 13-25). This benefit is entirely absent in Ikemasu, since formation of Ikemasu's opening 30 is insensitive to the selectability of the film layers 16, 17, and 18. Ikemasu provides no protection against mask misalignment and so provides no motivation to employ its more complex method for formation of the wordlines and bitlines of the BOI.

Ikemasu fails to teach depositing and leveling a third thick insulating layer selectively etchable with respect to the second insulating layer, as recited by claim 1. Ikemasu does not consider leveling any of the insulating layers disclosed. Rather, Figures 3B-3F of Ikemasu explicitly show all of the insulating layers 16, 17, 18, and 29 as not being leveled. This contrasts with Figures 3B-3D of the present invention which show the insulating layer as being leveled.

Claim 1 recites, "performing a chem-mech polishing." There is no teaching in the BOI or Ikemasu to perform such a step, nor is there any obvious motivation or suggestion to do so.

For at least the reasons listed above, the Background of the Invention in combination with Ikemasu fails to teach all the limitations of claim 1, which is therefore allowable thereover. Claims 2-8, as dependent claims on claim 1, are also allowable.

Claim 26 is allowable as dependent from claim 1. However, claim 26 is also allowable on its own merits, inasmuch as Ikemasu fails to teach depositing and leveling the third insulating layer after etching the second insulating layer, as recited by claim 26.

New dependent claims 27 and 28 also contain matter not disclosed by the BOI or Ikemasu, and are therefore allowable.

New claim 29 recites, in part, "depositing a second insulating layer, selectively etchable with respect to the first insulating layer, over the first insulating layer; etching a first opening in the second insulating layer above a portion of the active region of the substrate without exposing any portion of the first insulating layer directly above the wordline." Support for these limitations may be found in the specification beginning on page 7, line 19, and in Figures 3A and 3B. Claim 29 also recites, "depositing, after the etching step, a third insulating layer, selectively etchable with respect to the second insulating layer, over the first and second insulating layers; etching a second opening in the first and third insulating layers at the location of the first opening." Support for these limitations may be found in the specification at the previously cited text, as well as on page 8, beginning at line 7, and at Figure 3B and 3C.

A combination of Background of the Invention together with Ikemasu fails to teach these limitations. In contrast, Ikemasu teaches forming first and second silicon oxide film layers 16, 17, which are not selectively etchable with respect to each other (column 8, lines 52 and 53); teaches depositing a third layer 18 prior to etching of the second layer rather than after etching the second layer; and teaches forming a hole 30 that passes through the film layers 16, 17 and 18 without a previous etching step that opens the second layer (column 8, lines 63-67). Accordingly, claim 29 is allowable over the cited prior art. Dependent claims 30-37 are also therefore allowable.

Claim 30 recites etching a channel in at least the third insulating layer over the insulating trench, and depositing conductive material in the channel. Ikemasu fails to teach this limitation.

Claim 31 recites planarizing an upper surface of the third insulating layer, while claim 32 recites that the planarizing steps performed after the depositing conductive material step and includes removing conductive material from above the upper surface of the third insulating layer. Again, Ikemasu fails to teach or suggest any of these method steps.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative at (206) 622-4900 in order to expeditiously resolve prosecution of this application.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

Jérôme Ciavatti

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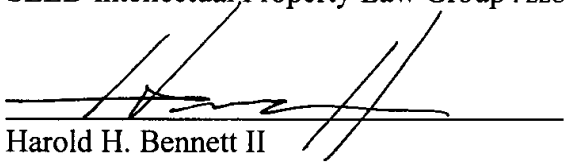

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